FIG. 1 (PRIOR ART)

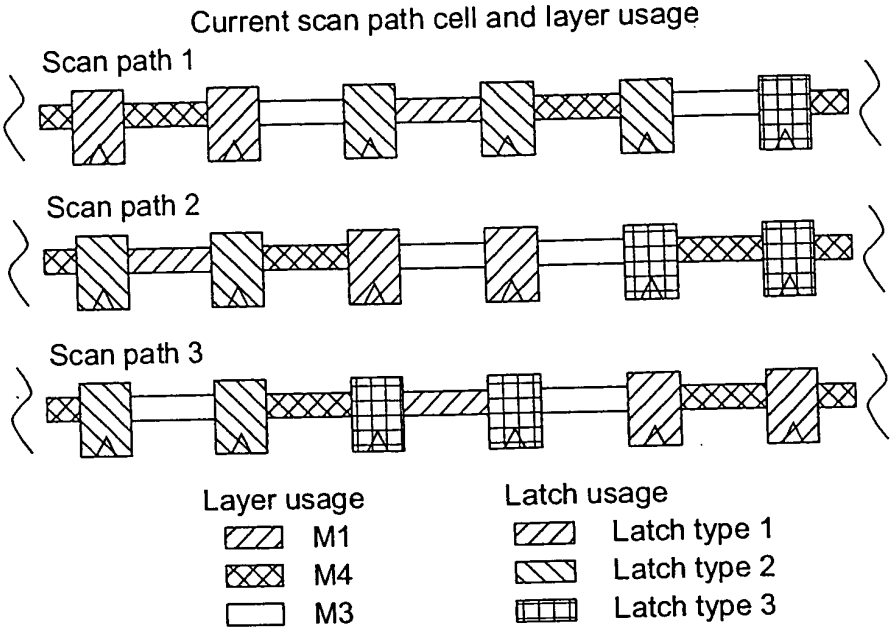


FIG. 2

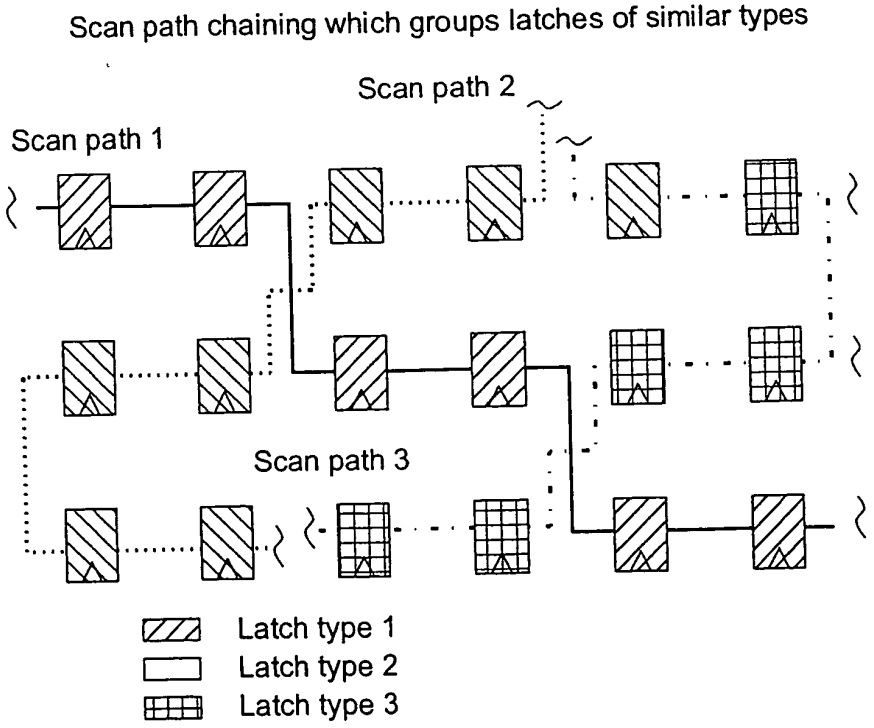


FIG. 3

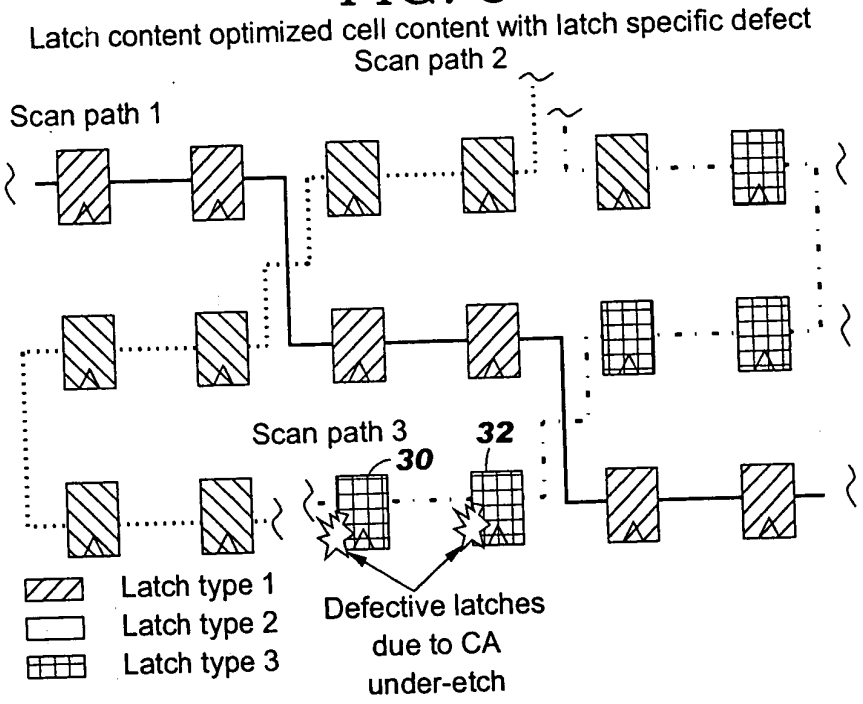

Latch content optimized cell content with latch specific defect
Scan path 2
Scan path 1
Scan path 3
32
30
Latch type 1
Latch type 2
Latch type 3
Defective latches
due to CA
under-etch

FIG. 4

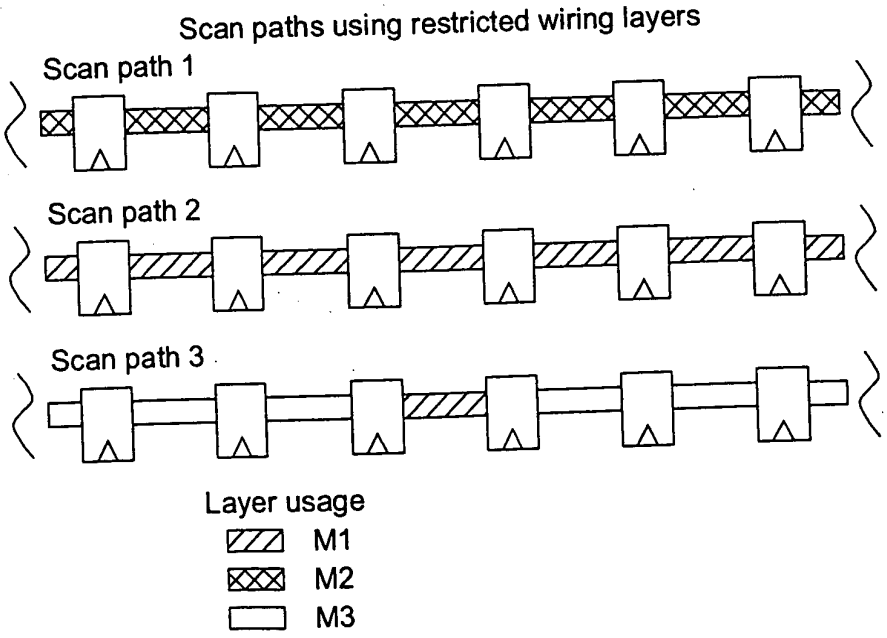
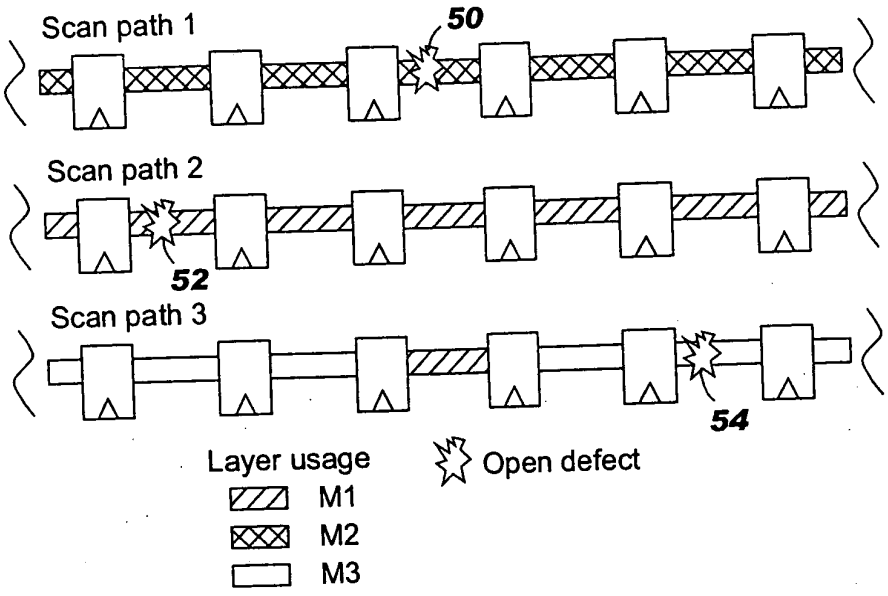

Scan paths using restricted wiring layers
Scan path 1
Scan path 2
Scan path 3
Layer usage
M1
M2
M3

FIG. 5

Layer optimized cell content with layer specific defects



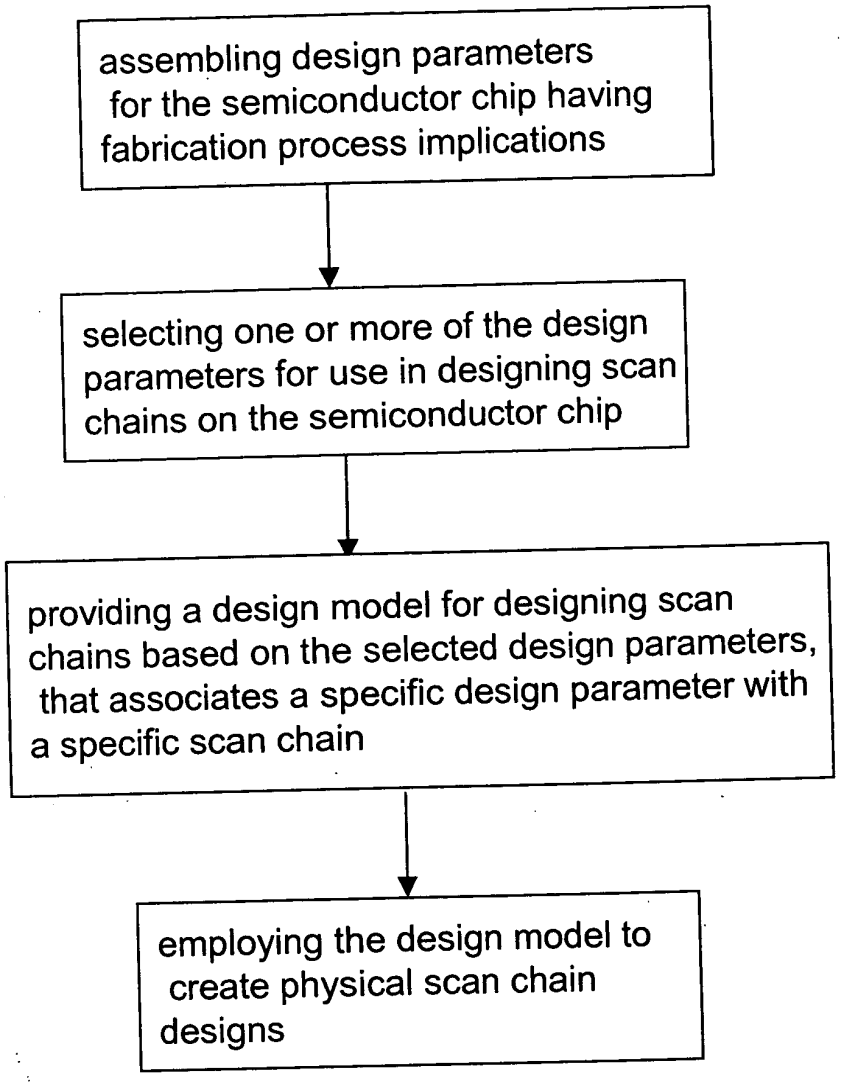

assembling design parameters for the semiconductor chip having fabrication process implications
selecting one or more of the design parameters for use in designing scan chains on the semiconductor chip
providing a design model for designing scan chains based on the selected design parameters, that associates a specific design parameter with a specific scan chain
employing the design model to create physical scan chain designs

Fig. 6

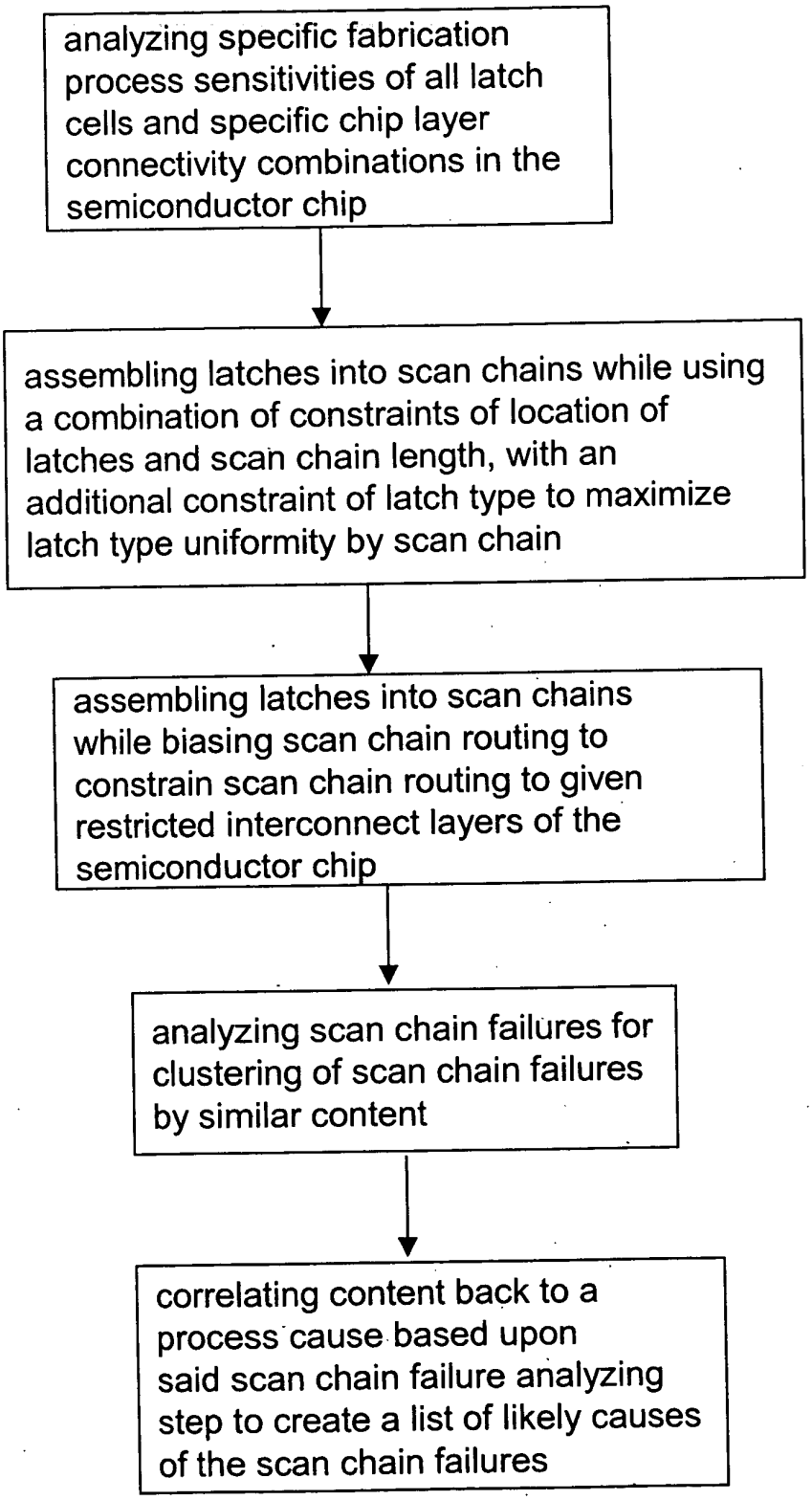

analyzing specific fabrication process sensitivities of all latch cells and specific chip layer connectivity combinations in the semiconductor chip
assembling latches into scan chains while using a combination of constraints of location of latches and scan chain length, with an additional constraint of latch type to maximize latch type uniformity by scan chain
assembling latches into scan chains while biasing scan chain routing to constrain scan chain routing to given restricted interconnect layers of the semiconductor chip
analyzing scan chain failures for clustering of scan chain failures by similar content
correlating content back to a process cause based upon said scan chain failure analyzing step to create a list of likely causes of the scan chain failures

Fig. 7

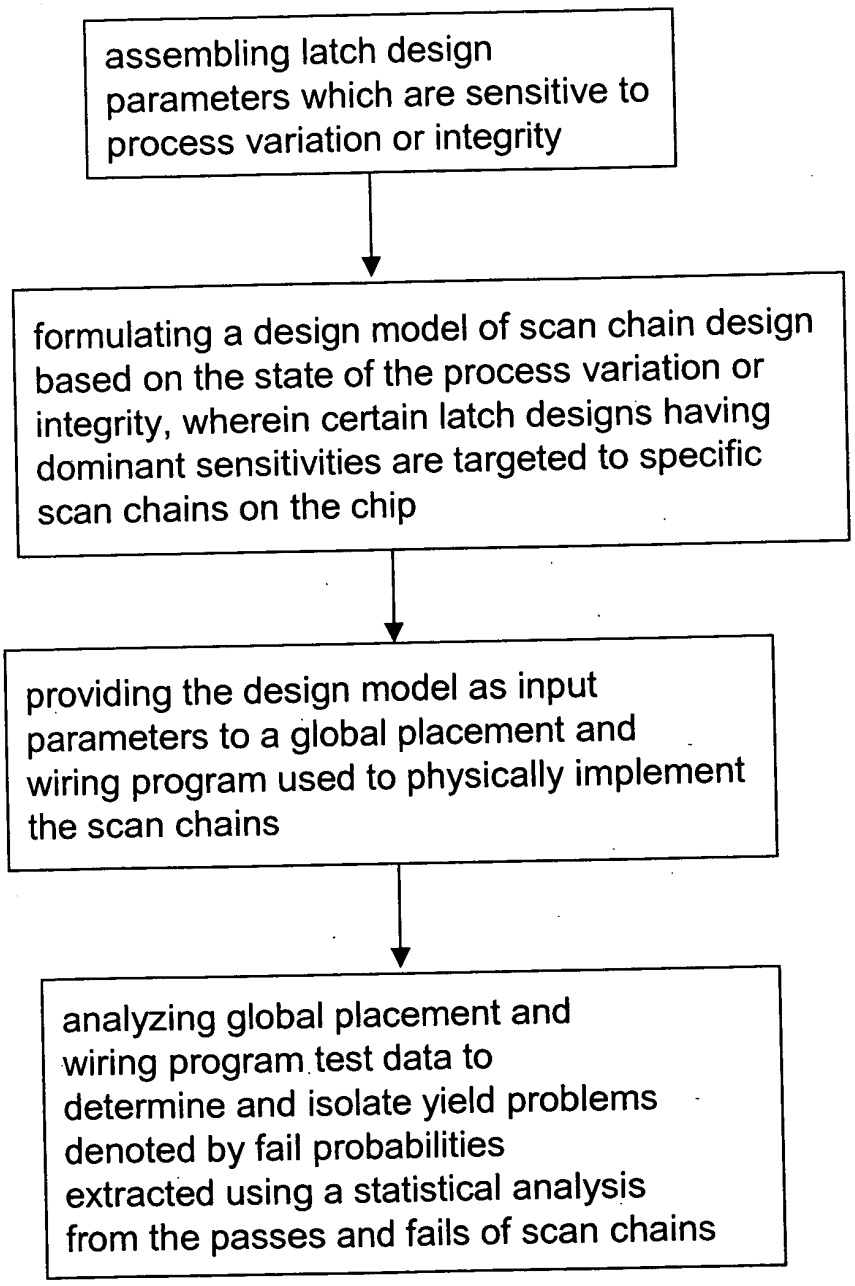

assembling latch design parameters which are sensitive to process variation or integrity
formulating a design model of scan chain design based on the state of the process variation or integrity, wherein certain latch designs having dominant sensitivities are targeted to specific scan chains on the chip
providing the design model as input parameters to a global placement and wiring program used to physically implement the scan chains
analyzing global placement and wiring program test data to determine and isolate yield problems denoted by fail probabilities extracted using a statistical analysis from the passes and fails of scan chains

Fig. 8